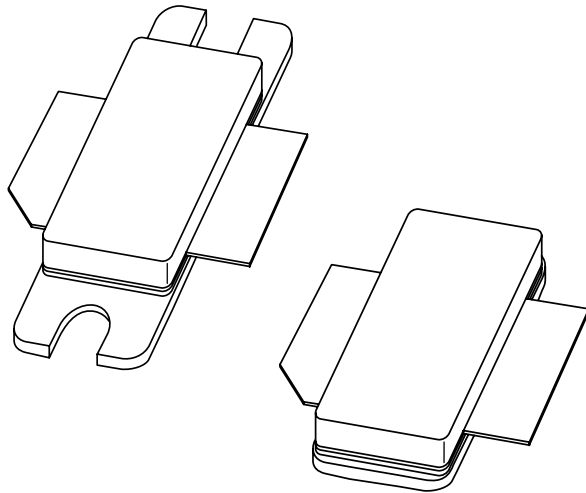


DATA SHEET



BLF0810-180; BLF0810S-180 Base station LDMOS transistors

Preliminary specification

2002 Aug 02

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

FEATURES

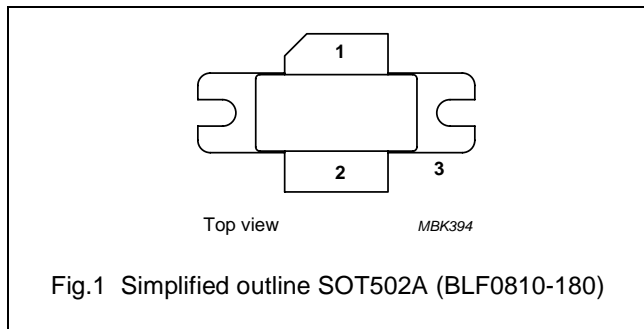
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1 GHz)
- Internally matched for ease of use.

APPLICATIONS

- Common source class-AB operation applicable in the 860 to 960 MHz frequency range
- CDMA and multi carrier applications.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



DESCRIPTION

180 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Typical CDMA IS95 performance at standard settings at a supply voltage of 28 V and $I_{DQ} = 1125$ mA, channel bandwidth is 30 kHz, adjacent channels at ± 750 kHz and at ± 1.98 MHz:

Output power = 35 W

Gain = 15.6 dB

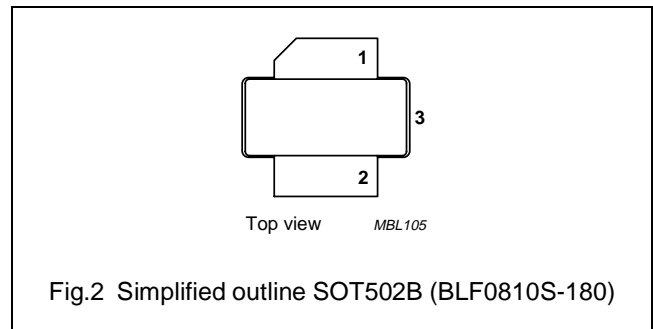
Efficiency = 26 %

ACPR <-45 dBc at 750 kHz and BW = 30 kHz

ACPR <-63 dBc at 1.98 MHz and BW = 30 kHz

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



QUICK REFERENCE DATA

Typical RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	d ₃ (dBc)	ACPR (dB)
Class-AB (2-tone)	f ₁ = 890.0 f ₂ = 890.1	28	140 (PEP)	15.2	35	-30	-
CDMA ⁽¹⁾	881.5	28	32	15.6	26	-	<-45 ⁽²⁾ <-63 ⁽³⁾
CDMA multi carrier signal ⁽⁴⁾	881.5	28	14	15.6	16	-	<-52 ⁽²⁾ <-56 ⁽³⁾

Note

1. IS95 CDMA (Pilot, Paging, Sync, and Traffic Codes 8 through 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz
4. 3 adjacent carriers with 32 channels walsh codes each.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	$T_h = 25\text{ °C}$, $P_L = 35\text{ W avg}$, note 1	<0.42	K/W
$R_{th\ hs-j}$	thermal resistance from heatsink to junction	$T_h = 25\text{ °C}$, $P_L = 32\text{ W avg}$, note 2	<0.62	K/W

Note

1. Thermal resistance is determined under RF operating conditions.
2. Depends of installation.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 3\text{ mA}$	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 300\text{ mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 36\text{ V}$	–	–	1	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GS(th)} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	45	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0$	–	–	1	μA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 10\text{ A}$	–	9	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 9\text{ V}$; $I_D = 10\text{ A}$	–	60	–	mΩ

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ }^\circ\text{C}$;

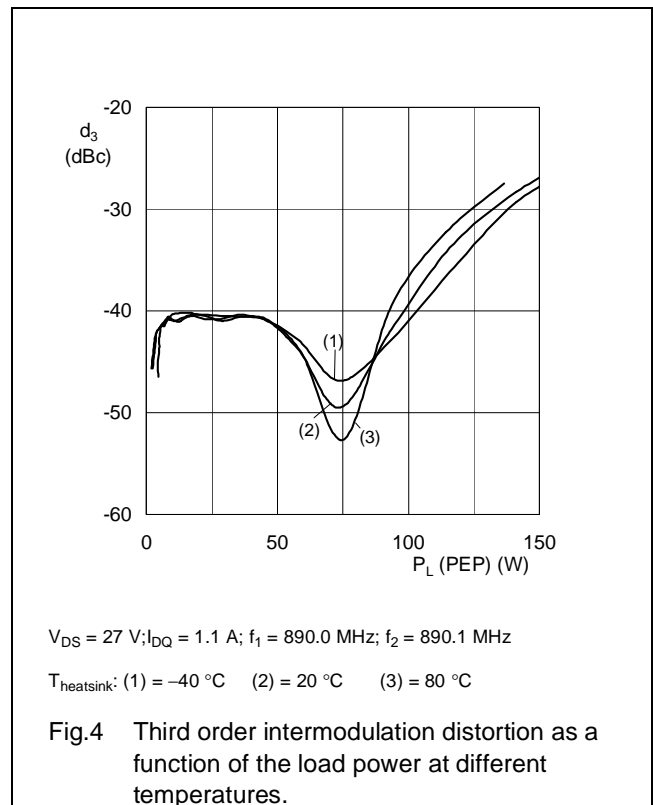
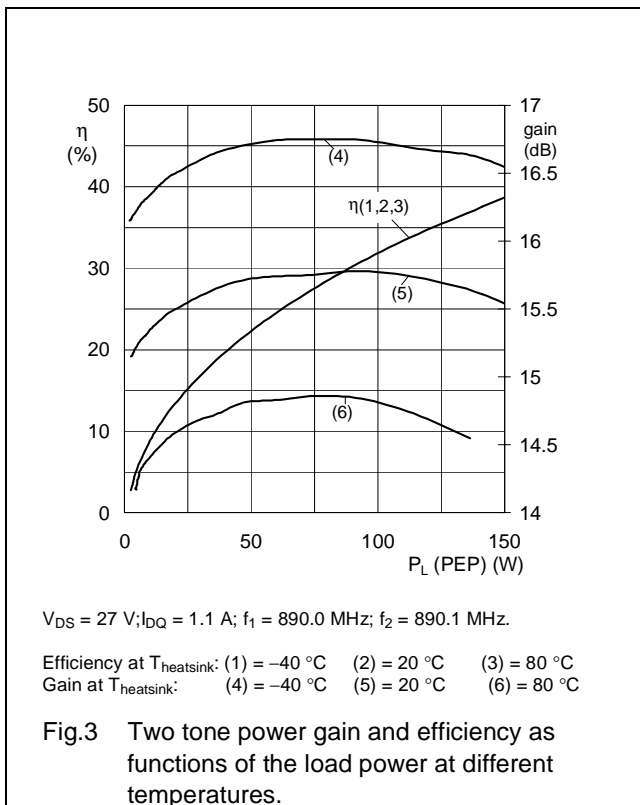
MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	I _{DQ} (mA)	G _p (dB)	η_D (%)	d ₃ (dBc)	ACPR (dB)
Class-AB (2-tone)	f ₁ = 890.0 f ₂ = 890.1	28	140 (PEP)	1125	15.2	35	-30	-
CDMA ⁽¹⁾	881.5	28	32	1250	15.6	26	-	<-45 ⁽²⁾ <-63 ⁽³⁾
CDMA multi carrier signal ⁽⁴⁾	881.5	28	14	1250	15.6	16	-	<-52 ⁽²⁾ <-56 ⁽³⁾

Note

- IS95 CDMA (Pilot, Paging, Sync, and Traffic Codes 8 through 13)
- ACPR 750 kHz at BW = 30 kHz
- ACPR 1.98 MHz at BW = 30 kHz
- 3 adjacent carriers with 32 channels walsh codes each.

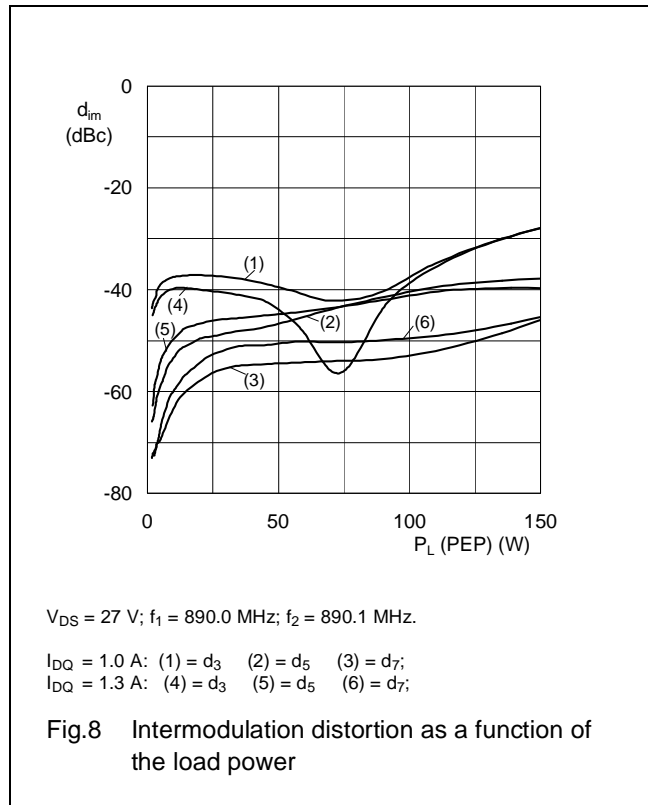
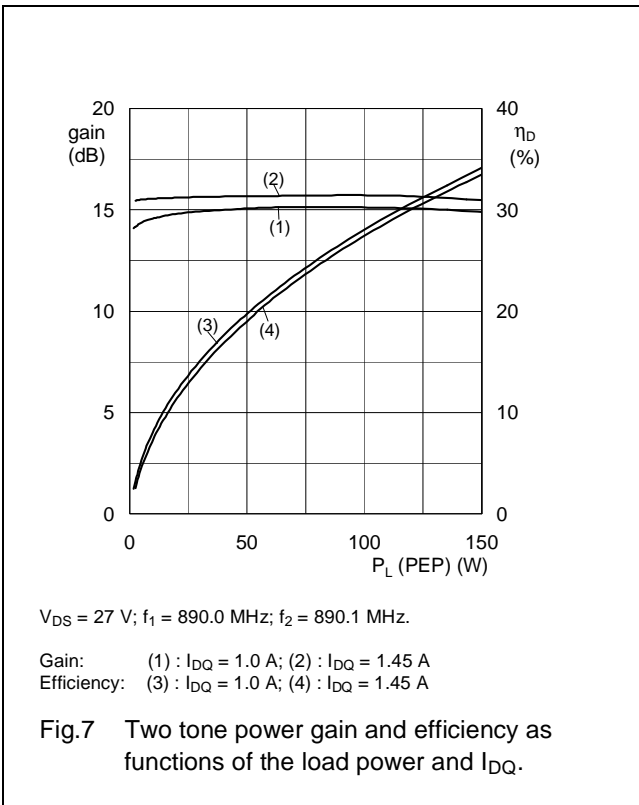
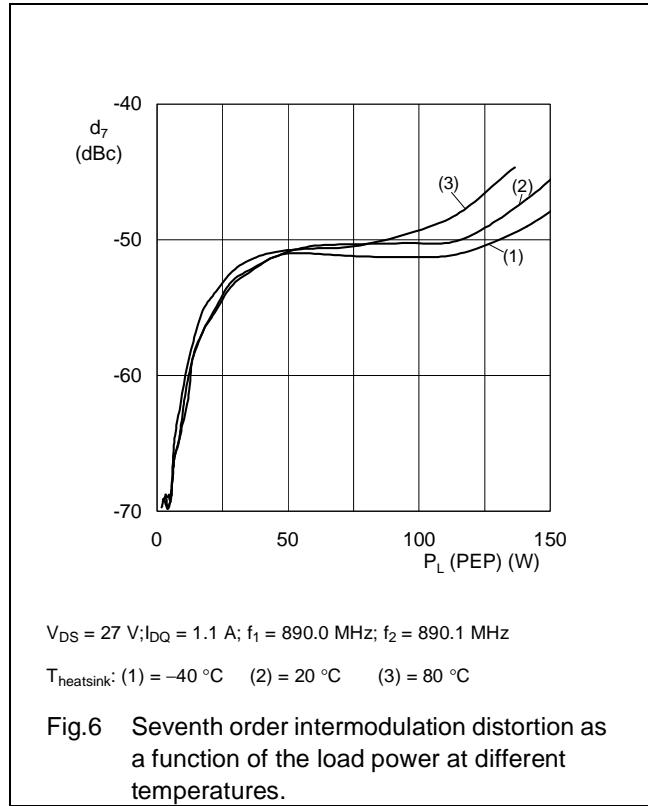
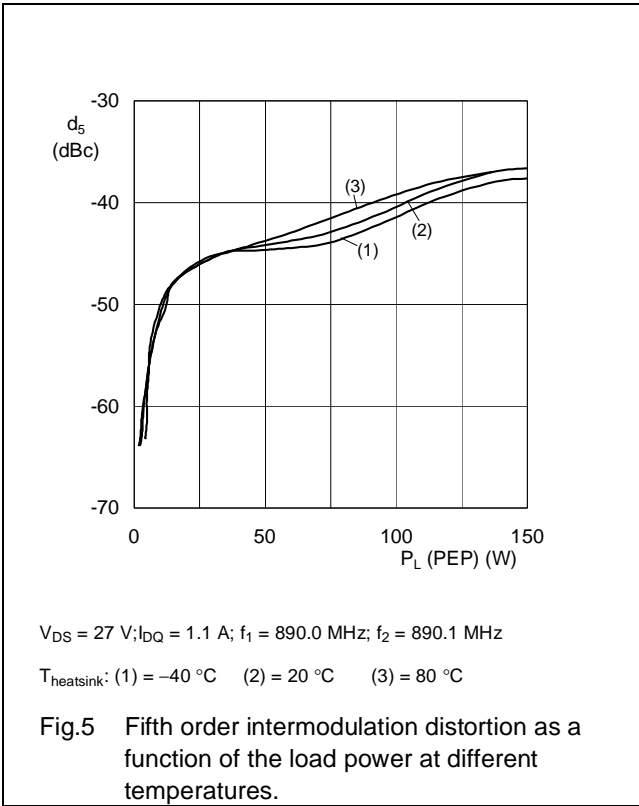
Ruggedness in class-AB operation

The BLF0810-180 and BLF0810S-180 are capable of withstanding a load mismatch corresponding to VSWR = 15 : 1 through all phases at V_{DS} = 27 V; P_L = 126 W (PEP).



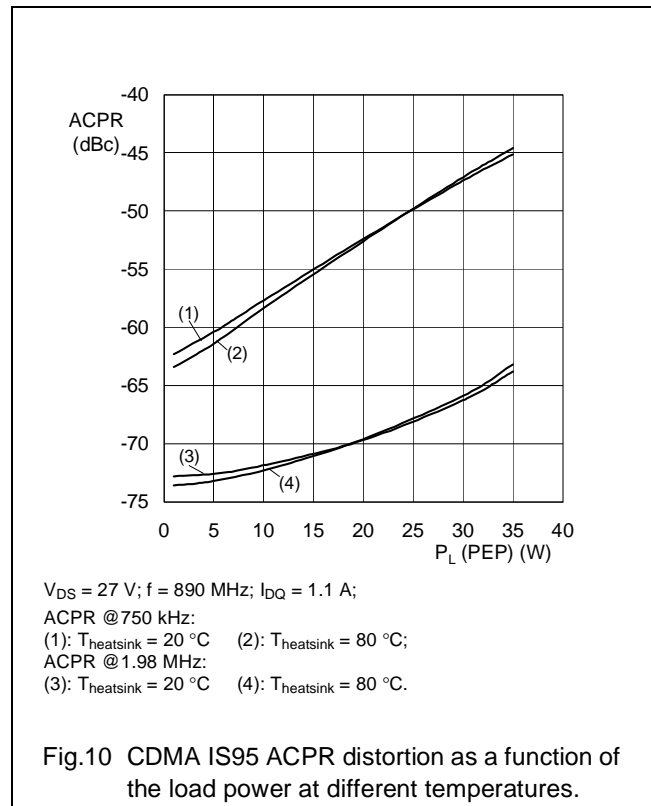
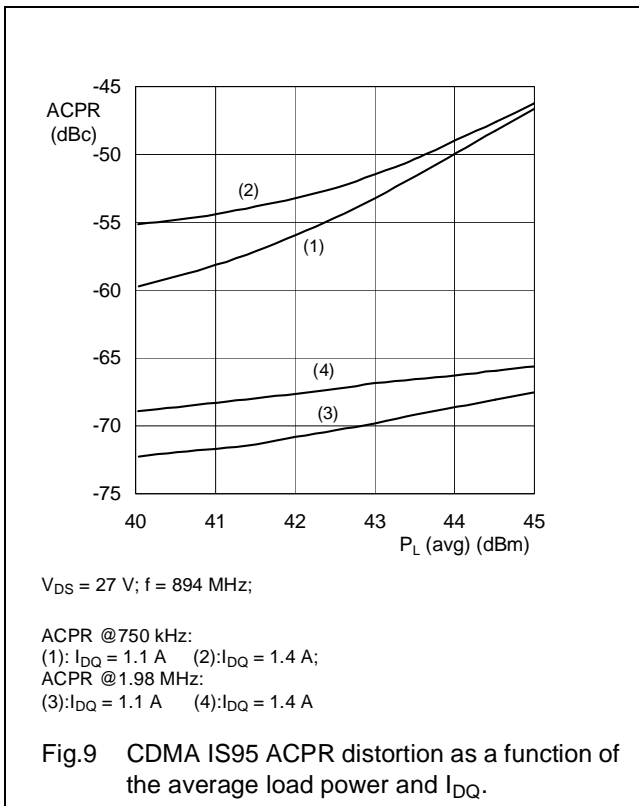
Base station LDMOS transistors

BLF0810-180; BLF0810S-180



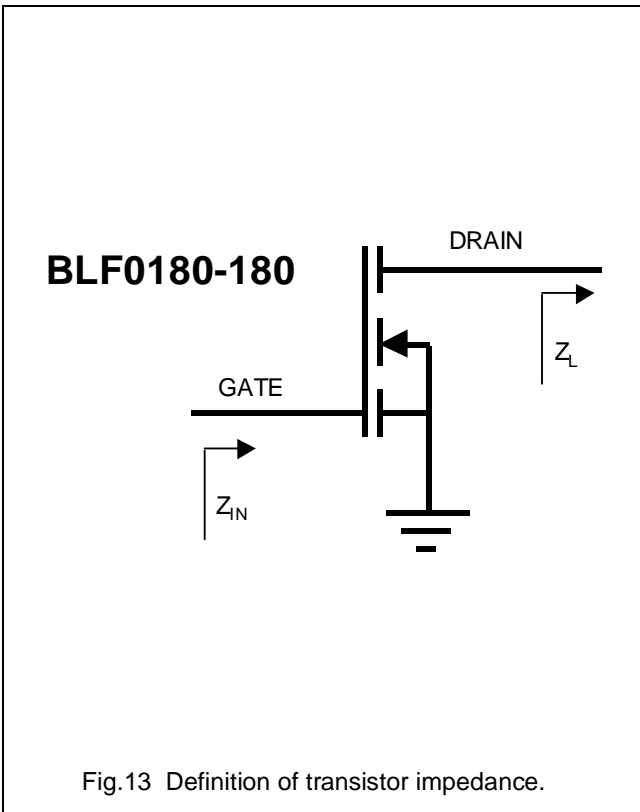
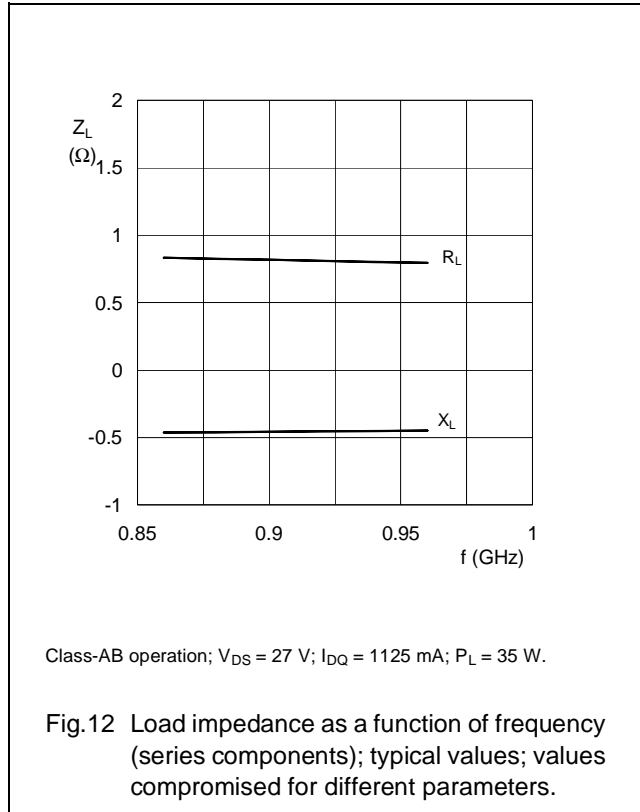
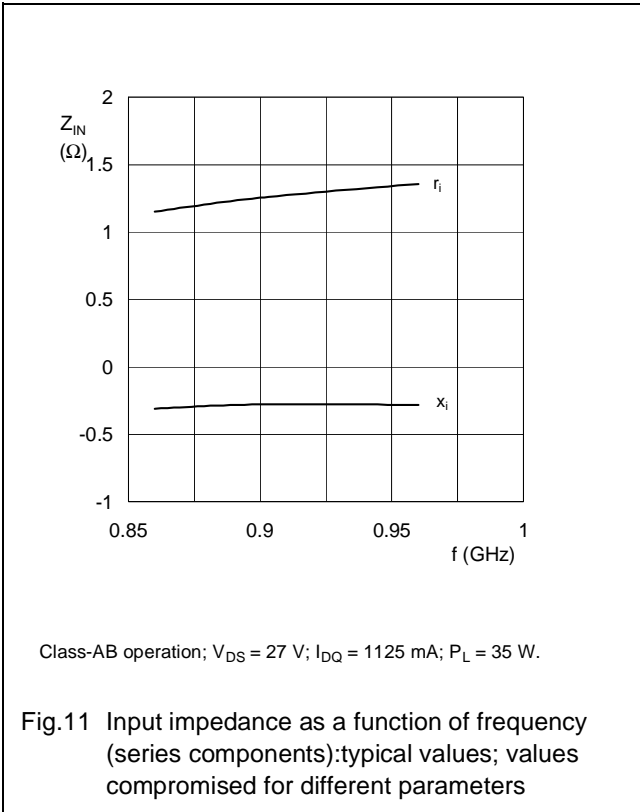
Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180

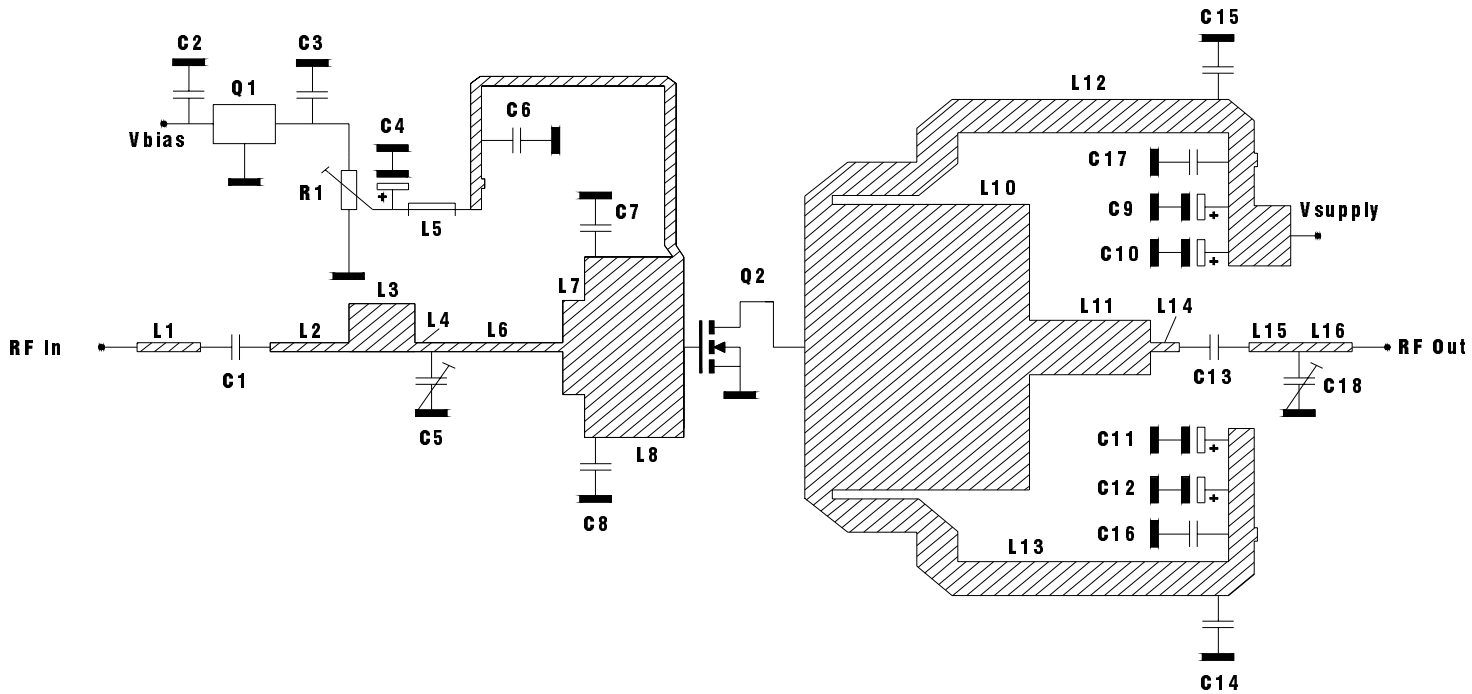
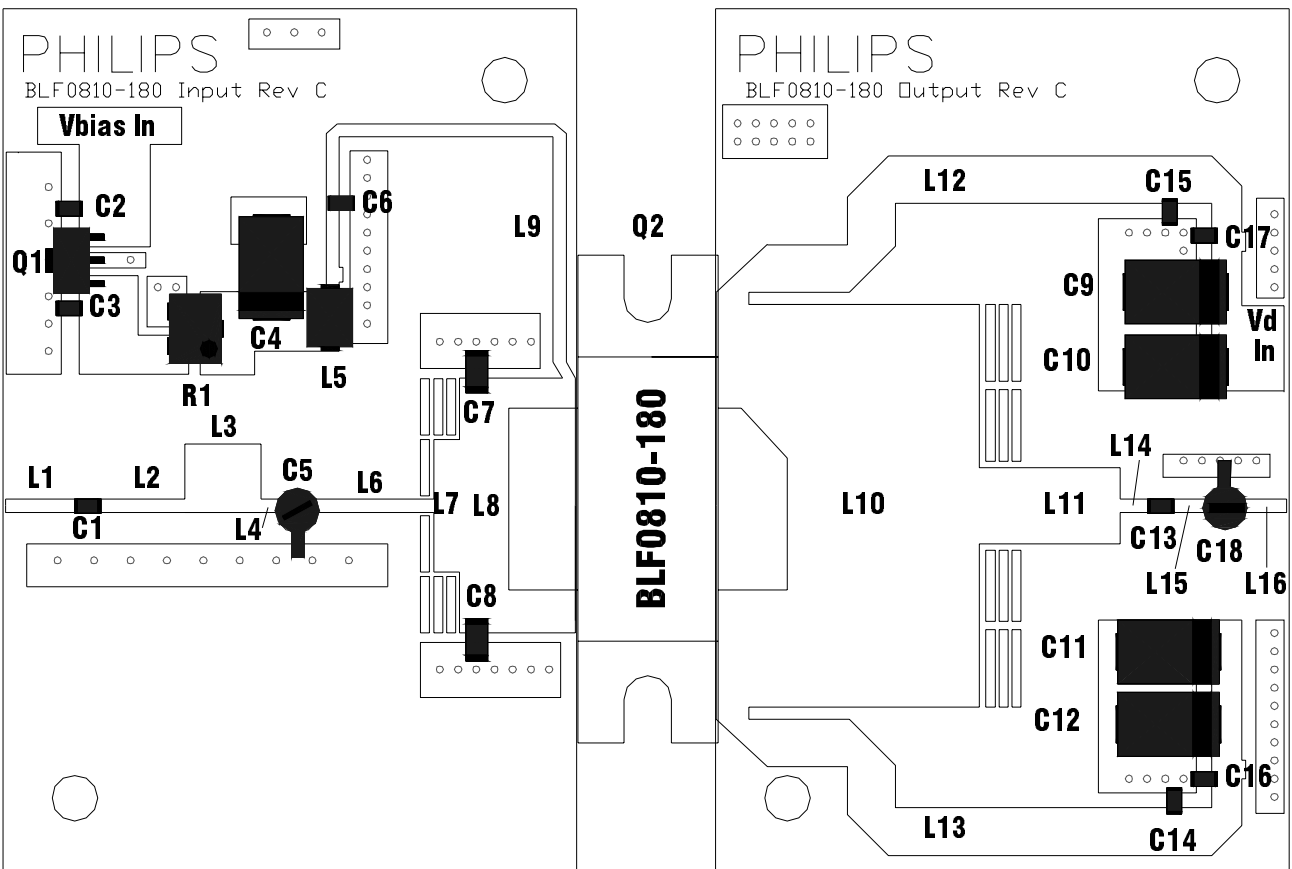


Fig.14 Circuit for 860 to 900 MHz test circuit.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 25 mils. The other side is unetched and serves as a ground plane.

Fig.15 Circuit for 860 to 900 MHz test circuit.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μ F	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 k Ω	
Q1	7808 voltage regulator		
Q2	BLF0910-140 LDMOS transistor		
L1	stripline; note 2		5.22 \times 0.92 mm
L2	stripline; note 2		6.47 \times 0.92 mm
L3	stripline; note 2		5.38 \times 4.8 mm
L4	stripline; note 2		2.4 \times 0.92 mm
L5	Ferroxcube		
L6	stripline; note 2		9.73 \times 0.92 mm
L7	stripline; note 2		1.82 \times 9.3 mm
L8	stripline; note 2		8.15 \times 17.9 mm
L9	stripline; note 2		44 \times 0.92 mm
L10	stripline; note 2		18.45 \times 28.3 mm
L11	stripline; note 2		9.95 \times 5.38 mm
L12, L13	stripline; note 2		37.6 \times 3.35 mm
L14	stripline; note 2		2.36 \times 0.92 mm
L15, L16	stripline; note 2		4.22 \times 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 0.64 mm

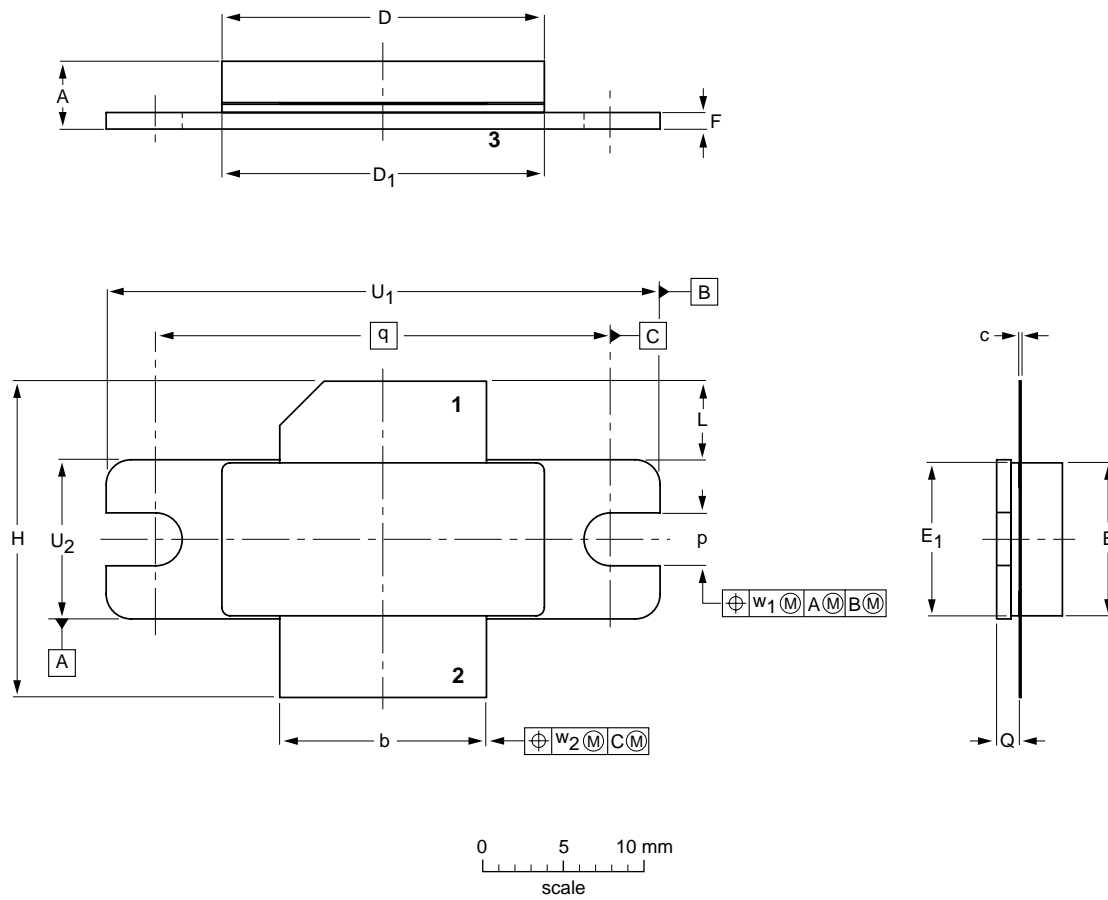
Base station LDMOS transistors

BLF0810-180; BLF0810S-180

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						-99-10-13- 99-12-28

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

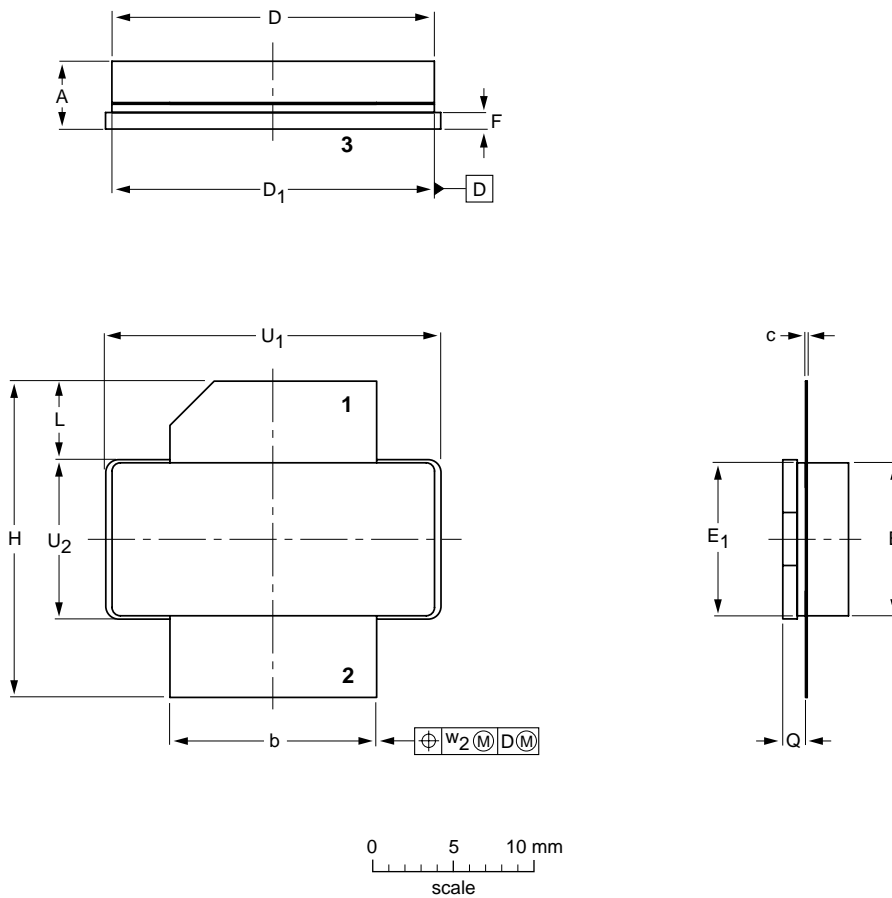
PACKAGE OUTLINE

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502B						99-12-16 99-12-28

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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